**Demonstrations**

1)Correctness of Line Block

2)Correctness of Arc Block

3)Correctness of Fill Color Function

4)Correctness of alpha blending of images

5)Correctness of splitting CPU instruction and four basic functional blocks response

6)AMBA AHB-Lite Protocol Interfacing

**Fixed Criteria**

1. (2 points) Test benches exist for all top-level components and the entire design. The test benches for the entire design can be demonstrated or documented to cover all of the functional requirements given in the design specific success criteria. - **READY TO DEMONSTRATE**
2. (4 points) Entire design synthesizes completely, without any inferred latches, timing arcs, and, sensitivity list warnings. - **TOP LEVEL NEEDS TO BE FIXED**
3. (2 points) Source and mapped version of the complete design behave the same for all test cases. The mapped version simulates without timing errors except at time zero. - **TOP LEVEL NEEDS TO BE FIXED**
4. (2 points) A complete IC layout is produced that passes all geometry and connectivity checks. - **READY TO DEMONSTRATE**
5. (2 points) The entire design complies with targets for area, pin count, throughput (if applicable), and clock rate. The final targets for these parameters will be determined by course staff based on your design review. Failure to reach any of the targets will result a score of 1 out of 2 provided that you are within 50% on area, 10% on pin count, and 25% on throughput. Doing worse in any category will result in a score of 0 out of 2. - **READY TO DEMONSTRATE**
6. Area: 4.0mm x 4.0mm
7. Pin Count: 210. 104 for AHB master and 104 for AHB slave + VCC and GROUND
8. Clock Frequency: 200 Mhz

**Design Specific Success Criteria**

1. (1 point) Demonstrate by simulation of a Verilog test bench that simple shapes, i.e. circle, triangle, circle can be drawn. - **READY TO DEMONSTRATE**
2. (1 points) Demonstrate by simulation of a Verilog test bench that the draw line and arc functional blocks work correctly – **READY TO DEMONSTRATE**
3. (2 points) Demonstrate by simulation of a Verilog test bench that the AHB bus can transmit data as expected. - **READY TO DEMONSTRATE**
4. (1 point) Demonstrate by simulation of a Verilog test bench that colors can be filled into the shapes. - **READY TO DEMONSTRATE**
5. (1 point) Demonstrate by simulation of a Verilog test bench that alpha blending of images work correctly. - **READY TO DEMONSTRATE**
6. (2 point) Demonstrate by simulation of a Verilog test bench that Control unit, Drawshape, Decoder and FIFO split instructions correctly. - READY TO **DEMONSTRATE**